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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/798,994	03/11/2004	Jeffery Steven Beck	10030326-1	6851
68551	7590	09/19/2008		
RatnerPrestia P.O. BOX 980 VALLEY FORGE, PA 19482			EXAMINER NGUYEN, LUONG TRUNG	
			ART UNIT 2622	PAPER NUMBER
			MAIL DATE 09/19/2008	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/798,994	Applicant(s) BECK ET AL.	
	Examiner LUONG T. NGUYEN	Art Unit 2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 19 June 2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-5 and 7-16 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-5, 7-16 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 6/19/2008 has been entered.

Response to Arguments

2. Applicant's arguments filed on 4/10/2008 have been fully considered but they are not persuasive.

In re page 5, Applicants argue that Borg et al. does not disclose or suggest “a reference circuit that generates a unique reference voltage associated with each pixel in each row of pixels.”

In response, regarding claim 1, Applicants amended claim 1 with limitation “a reference circuit that generates a unique reference voltage associated with each pixel in each row of pixels.” The examiner considers that Borg et al. does disclose this limitation. Borg et al. discloses reference column amplifier 240, which generates a unique voltage associated with each pixel 10 in each row of active pixel sensor array 280 when the timing controller select which row to read out (figure 3A, column 6, lines 17-60). It is noted that the reference column amplifier 240 is associated to pixels 10 of active pixel sensor array 280.

In re page 6, Applicant argue that Borg does not suggest a reference amplifier that samples and holds the unique reference voltage for each one of the pixels in the groups (or columns) and rows of pixels.

In response, Applicants amended claim 1 with limitation “the reference amplifier samples and holds the unique reference voltage for each one of the pixels in the groups and rows of pixels.” The examiner considers that Borg et al. does disclose this limitation. Borg et al. discloses reference column amplifier 240, which samples and holds a unique voltage for each pixel 10 in each row of active pixel sensor array 280 when the timing controller 200 selects which row to read out (figure 3A, column 6, lines 17-60; column 4, lines 15-29). It is noted that the reference column amplifier 240 is associated to pixels 10 of active pixel sensor array 280.

In re page 6, Applicants argue that Borg et al. does not disclose or suggest “a reference circuit that samples and holds a unique reference voltage as each video voltage is read from the video circuits” as amended in claims 5, 10 and similar in method claim 13.

In response, regarding claim 5, Applicants amended claim 5 with limitation “a reference circuit that samples a unique reference voltage as each video voltage of each pixel in a row of pixels is read.” The examiner considers that Borg et al. does disclose this limitation. Borg et al. discloses reference column amplifier 240, which samples and hold a unique voltage as each video voltage of each pixel is read when the timing controller 200 selects which row to read out (figures 3A, column 4, lines 15-29; column 6, lines 17-60).

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3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-5, 7-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Borg et al. (US 6,476,864).

Regarding claim 1, Borg et al. discloses an active pixel sensor array sampling system comprising:

a video circuit (column amplifiers 230, figure 3A, column 6, lines 17-60) that generates a video voltage from each one of a group of pixels in each column of pixels;

a reference circuit (reference column amplifier 240, which generates a unique voltage associated with each pixel 10 in each row of active pixel sensor array 280 when the timing controller select which row to read out. It is noted that the reference column amplifier 240 is associated to pixels 10 of active pixel sensor array 280, figure 3A, column 6, lines 17-60) that generates a unique reference voltage associated with each pixel in each row of pixels; wherein the video circuit comprises a plurality of video amplifiers (column amplifiers 230, figure 3A, column 6, lines 17-60), each video amplifier being associated with a respective one of the pixels in the group of pixels (each amplifier 230 associated with each pixel 10 on each column line 38, figure 3A, column 6, lines 17-60), the reference circuit comprises a single reference amplifier (reference column amplifier 240, figure 3A, column 6, lines 17-60) associated with all of the pixels in the groups and rows of pixels, and wherein the reference amplifier samples and holds

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the unique reference voltage for each one of the pixels in the groups and rows of pixels (column 4, lines 15-29).

Regarding claim 2, Borg et al. discloses wherein each of the video amplifiers is associated with all of the pixels in a respective column of pixels (each amplifier 230 associated with each pixel 10 on each column line 38, figure 3A, column 6, lines 17-60).

Regarding claim 3, Borg et al. discloses a differential amplifier (differential image signal 118, figures 3A, 4, column 6, lines 45-60) that generates a differential voltage responsive to the video voltage and the unique reference voltage associated with each pixel.

Regarding claim 4, Borg et al. discloses the reference amplifier has an output continuously coupled to the differential amplifier during reading of the video voltage of each of the video amplifiers (figures 3A, 4, column 6, lines 17-60).

Regarding claim 5, Borg et al. discloses an active pixel sensor array sampling circuit that samples a voltage on each one of a plurality of pixels, the circuit comprising:

a plurality of video circuits (column amplifiers 230, figure 3A, column 6, lines 17-60), each video circuit generating a video voltage related to a voltage on a respective one of the pixels as its respective pixel is sampled;

a reference circuit (reference column amplifier 240, figure 3A, column 4, lines 15-29,

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column 6, lines 17-60) that samples a unique reference voltage as each video voltage is read from the video circuits;

wherein the pixels are arranged in columns and rows, wherein the reference circuit is associated with all of the pixels of each row of pixels, and the reference circuit samples and holds a unique reference voltage as each video voltage of a row of pixels is read (figure 3A, column 4, lines 15-29, column 6, lines 17-60).

Regarding claim 7, Borg et al. discloses a differential amplifier (differential image signal 118, figures 3A, 4, column 6, lines 45-60) that provides a differential voltage representing a difference between each read video voltage and each sampled unique reference voltage.

Regarding claim 8, Borg et al. discloses wherein the reference amplifier has an output continuously coupled to the differential amplifier during the reading of the video voltages for each row of pixels (figures 3A, 4, column 6, lines 17-60).

Regarding claim 9, Borg et al. discloses wherein each video amplifier is associated with all of the pixels of a respective column of pixels (each amplifier 230 associated with each pixel 10 on each column line 38, figure 3A, column 6, lines 17-60).

Regarding claim 10, Borg et al. discloses an integrated circuit including an active pixel sensor array sampling system comprising:

a plurality of video circuits, each video circuit sampling a video voltage from each one of

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a group of pixels in each column of pixels (column amplifiers 230, figure 3A, column 4, lines 15-29, column 6, lines 17-60);

a reference circuit (reference column amplifier 240, figure 3A, column 4, lines 15-29, column 6, lines 17-60) that samples a unique reference voltage for each pixel in a row of pixels, as each video voltage is read from the video circuits.

Regarding claim 11, Borg et al. discloses a differential amplifier (differential image signal 118, figures 3A, 4, column 6, lines 45-60) that generates a differential voltage responsive to each read video voltage and its corresponding sampled unique reference voltage.

Regarding claim 12, Borg et al. discloses wherein the pixels are arranged in columns and rows and wherein each video circuit is associated with all of the pixels of a respective column of pixels (figure 3A).

Regarding claims 13, 14, 16, claims 13, 14, 16 are method claims of apparatus claims 10-12, respectively. Therefore, claims 13, 14, 16 are rejected for the reasons given with respect to claims 10-12.

Regarding claim 15, Borg et al. discloses steps of arranging the pixels in plural groups (group of pixels 10 are arranged on each column 38, figure 3A), and providing a single reference (reference amplifier 240, figure 3A, column 6, lines 35-60) amplifier for all of the groups of pixels.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to LUONG T. NGUYEN whose telephone number is (571) 272-7315. The examiner can normally be reached on 7:30AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID L. OMETZ can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

LTN
9/14/08

/LUONG T NGUYEN/
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